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ANALYSIS OF DIGITAL LOGIC CIRCUITS BASED ON CNTFET

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ABSTRACT

This paper addresses at first carbon NanoTubes (CNTs) and importance of CNT over silicon based devices has been discussed and then exploring the recent survey on CNTFET structure. In this work, the performance of carbon Nanotube field effect transistors is evaluated and analysis by using digital logic circuit. We know that CNT had proposed as alternative to silicon CMOS technology.CNT having two types that are one is MOSFET type and other one is Schottky-barrier(SB).both types of CNT conduct electron and holes to showing a p-type and n-type behavior. In this model CNTFET based devices offer high mobility for near ballistic transport and high carrier velocity for fast switching. CNFET based device offering molecular devices of technology that the convention CMOS device leaves off. CNTFET could be more achievable devices in comparison to other nanotechnology. After realization of high performance of device CNTFET using basic logic circuit, use SB-CNTFET to design basic logic circuits.

Keywords- CNFET (carbon nanotube field effect transistor), CMOS (complementary metal oxide semiconductor), CNT (carbon NanoTubes), P-G (polarity gates), SWNT (single wall Nanotube), MWNT (multi wall Nanotube), CGD (gate to drain capacitance), SB (Schottky barrier).

I. INTRODUCTION

Until the mid-1980's pure solid carbon were thought to exist on only two physical forms, diamond and graphite. Diamond and graphite have different physical structures and properties, both atoms are arranged in covalently bonded networks. These two different physical forms of carbon atoms are Called allotropes. The unique geometric properties of this new allotrope of carbon did not end at soccer shaped molecules, it was also discovered that carbon atoms can form long cylindrical tubes. These tubes were called "bulky tubes" but better known as Carbon nanotubes or CNT for short Carbon nanotubes is most of the promising candidates that replace CMOS technology. CNTs provide excellent property like high carrier velocity, near quasi ballistic transport, high carrier mobility (10^3-10^4) and easily integration of highly-k material, fabrication, design and gives better result electrostatics. CNT is graphene strips rolled up into tubular shapes with cylindrical nano structure. Carbon NanoTubes observed by Iijima 1991 in Tokyo.

Carbon nano tubes are highly resistant to electro migration and it's also enable optical emission. All carbon bonds are well satisfied with the surface of carbon nanotube, which results oxides interfaces. In this work we developed the logic circuit of using CNFET, today's silicon based MOSFET technology size less than 1-nm to 50nm are common to the world of electronics.

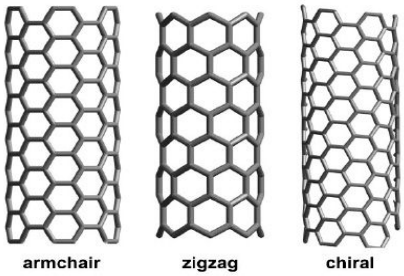

Fig1. (a) Armchair CNT, fig (b) zigzag CNT, fig(c) chiral CNT

Further, scaling has faced serious limits relate to fabrication technology and designing. Other solution involve using silicon MOSFET high-k dielectric material useful for gate insulator channel and reduce direct tunneling to leakage currents. Therefore, I-V characteristics of CNFET as that of CMOS circuit will be design using logic circuit based CNFET.

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II. LITERATURE REVIEW

A. CARBON NANOTUBES

CNTs exhibit extraordinary strength unique thermal electrical and mechanical properties. Nanotubes is categorized as single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs).Most single-walled nanotubes (SWNTs) have a diameter of close to 1 nanometer, with a tube length that can be many millions of times longer. Here first intermolecular logic gates using SWCNT FETs was made in 2001. A logic gate requires both a p-FET and an n-FET. Because SWNTs are p-FETs when exposed to oxygen and n-FETs otherwise, it is possible to protect half of the SWNT from oxygen exposure, while exposing the other half to oxygen. Multi-walled nanotubes (MWNTs) consist of multiple rolled layers of graphene. There are two models that can be used to describe the structures of multi-walled nanotubes .The nanotubes act as Electrodes and allow the storage devices to conduct electricity. A semiconductor carbon nanotube seems to be appropriate to be used as the channel of field effect transistors. A carbon nanotube field-effect transistor (CNTFET) refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure.

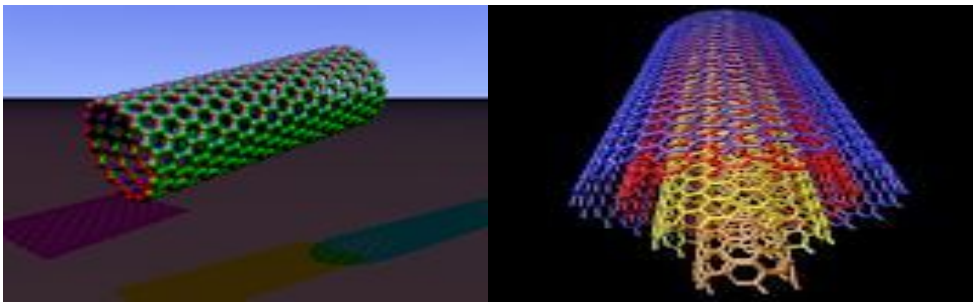

Fig: 2 (a) SNWN and fig: (b) MNWT

Diameter of CNT can be calculated as the following as

$$D_{CNT} = \sqrt{3}a\frac{\sqrt{P^2+PQ+Q^2}}{\pi} \quad (1)$$

CNT is expressed in terms of a chiral vector

$$c_N = p_{a1+}q_{a2} \quad (2)$$

That connects two dimension graphene sheets, where p and q are integer index and a^1 and a^2 are unit vector.

Therefore, the structure of any carbon nanotube can be index (p, q) is metallic when p= q has semiconducting and

P-q=3i

Where,

I= integer,

P - q≠3i semiconducting.

The threshold voltage of the intrinsic CNT channel can be approx of first order as the half band-gap is an inverse function of the diameter.

B. BASIC CNTFET

The first CNTFET was reported on 1998.The Carbon Nanotubes had been identified with an excellent choice of next generation of field-effect transistors, which maintain the operating principles of the currently used devices, but replace the conducting channel with carbon nano materials such as one-dimensional (1D) CNT or two-dimensional (2D) graphene layers. Carbon nanotube field effect transistor (CNTFET) uses CNT as of semiconducting channels.

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Today CNTFETs are regarded as an important contending device to replace conventional silicon transistors. CNTFETs are typically p-type devices that operate on so-called Schottky barrier (SB) transistors. The p-type characteristics have been attributed to the alignment of source-drain. Early CNTFETs were fabricated from oxidized silicon substrates with a back-gated geometry and a thick SiO2 layer that resulted in poor gate control of drain current the use of a top-gated geometry produced immediate performance improvements metal Fermi level near the valence band of the CNTs rather than to background doping or charges. The possibility of ballistic operation of CNTFETs has been a topic of great interest. As the mentioned above CNT are used in CNFET as channel and it's also depending on the connection between source and drain.

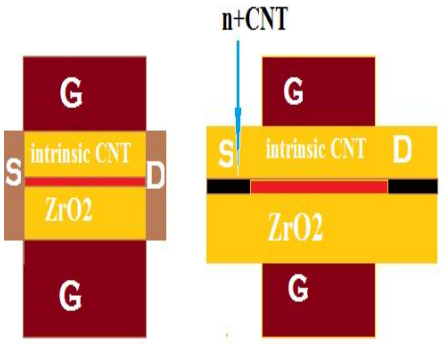

Fig.3. Different types of CNTFETs: (a) Schottky barrier CNTFET (b) MOSFET-like CNTFET.

CNTFETs provide a unique property to control threshold voltage by the changing in chirality vector, and the diameter of the CNT. The threshold voltage of both P-CNTFET and N-CNTFET obtained from simulation for various chirality vectors. Comparison of CNTFET-based logic circuits of CMOS logic circuits is necessary to establish means of evaluation for performance metrics such as current density, device switching speed, propagation delay through the gates, switching energy, operating temperature, and cost.

However, the technology is not sufficiently mature to enable meaningful comparisons between the positioning techniques, must still evolve to enable high-yield volume manufacturing and contact technology must be improved to reduce the impact of contacts on circuit performance.

III. PROPOSED MODEL

There is Different types of CNTFET have been demonstratively in the literature. We know there are mainly two types of CNTFET: Schottky barrier CNTFET (SB-CNTFET) and MOSFET-like CNTFET as shown Fig. 1. In SB-CNTFET the channel is made of intrinsic semiconducting CNT and directs contacts of the metal with the semiconducting nanotubes are made for source and drain regions. The principle of working of device direct tunneling through the Schottky barrier (SB) at the source-channel junction. The application of gate voltage is modulated by the barrier-width and thus, the transconductance of the devices is controlled by the gate voltage.

In MOSFET-like CNTFET doped CNTs are used for the source and drain regions and channel are made of intrinsic semiconducting CNT. In this work we use the SB-CNTFETs to design basic logic circuits. In SB-CNTFET the channel is made of intrinsic semiconducting CNT and direct contacts of the metal with the semiconducting nanotubes are made for source and drain regions.

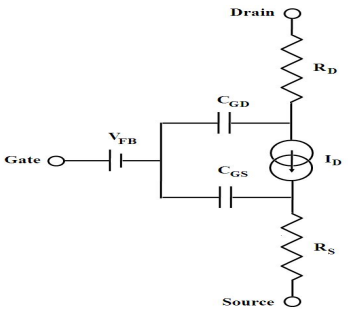

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Fig.4. Schematic of SPICE compatible CNTFET model, where CGS is gate to source capacitance, CGD is gate to drain capacitance, RD is drain resistance, RS is source resistance, VFB is flat-band voltage, and ID is drain current.

- First of all realization of high performance digital circuits using CNTFET.
- This model is applicable to arranging of CNTs with diameter 1 to 3nm and the evaluated the drain current I_D and total current channel Q_{CNT} is illustrated in figs.
- In this model surface potential $_s$ and the specific voltage $_1$(S/D) is mainly used the sub band energy level p and μS/D source Fermi level.
- Now, the specific voltage is given by

$$\xi_I = \frac{\psi s - \Delta p - \mu i}{KBT} \qquad (3)$$

Where,

I=source and drain

K_B= Boltzmann constant

T =operating temperature

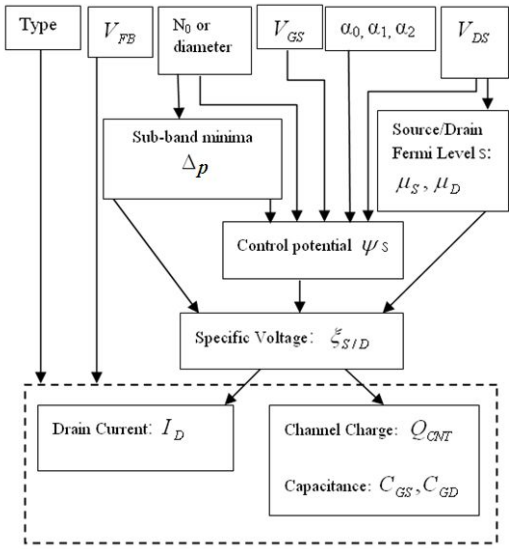

Fig.5. Structure of CNTFET compact model

- If conduction bands will be minima for sub band is set to half nanotube band gap Δp and p^{th} equilibrium conduction bands minima Δp is given by,

$$\Delta p = \frac{\Delta 1[6p - 3 - (-1)p}{4} \qquad (4)$$

- This models formation is to get the control potential for with gate bias voltage.

V_{GS}-ψs=0 for $V_{GS}<\Delta 1$

= α($V_{GS}<\Delta 1$) for $V_{GS}>\Delta 1$

- α is a parameter and given by

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$\alpha = \alpha_0+\alpha_1 V_{DS} +\alpha_2 V^2_{DS}$ (5)

Where,

α_0 , α_1, α_2 = depend CNT & gate oxide thickness

Then,

I_D is given by,

$$I_D = \frac{4eKBT}{h} \Sigma p[In(1+e^{-\varepsilon s}) - In(1+e^{-\varepsilon d}) \quad (6)$$

Where,

P= no. of substance

e= charge of electron

h= planks constant

I_D= drain current

- The gate biased voltage required to produce the assuming s based electrostatic .capacitance is given by

$$\psi s = V_G - Q_{NT}/C_{INS} \quad (7)$$

Where, C_{INS} = insulator capacitance

Since, in this way we obtained simplified models of CNTFET and p-type and n-type CNTFET can be obtained only alternating the polarity gate (PG).

A. CNTFET- BASED LOGIC CIRCUITS

In this section we have to describe the different components for that conforms our overall design flow for CNFET-based logic circuits. We design an inverted circuit using based on CNTFET pull up network is implemented (PUN) USING P-TYPE CNTFET pull downs network(PDN) Is implemented using n-type CNTFET.

The voltage transfer characteristics of CNTFET inverter as shown in fig. shift transition to two sheets with threshold voltage equal to half power supplies. And the simulation result shown in figs. in this waveform there is two logic declarations in the both logic 0 and logic 1.the propagation delay with through the gate, dynamic power and power delay dissipation.

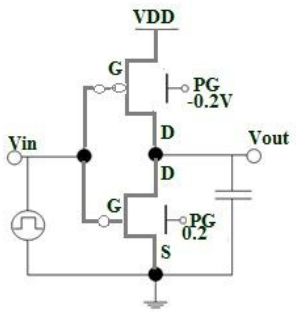

Fig. 7: CNTFET inverter

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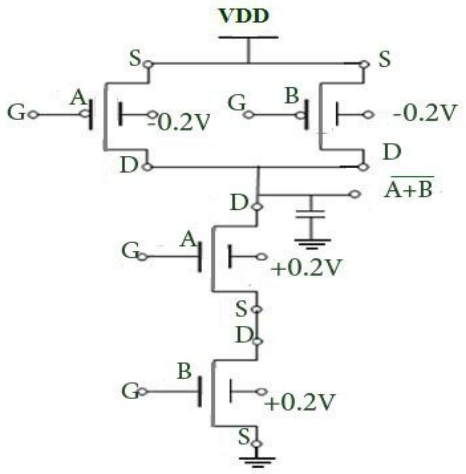

Fig.8: Two inputs NAND gate using CNTFET.

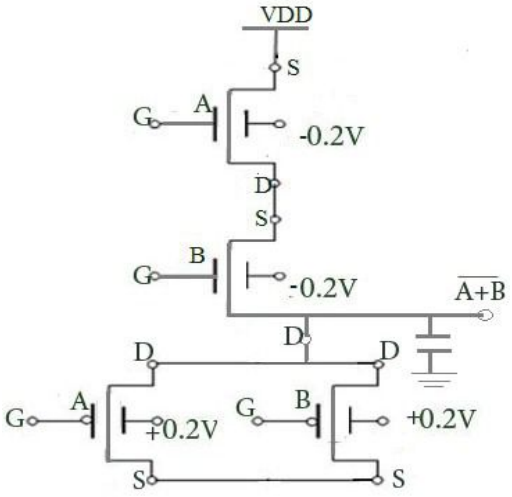

Fig.9: Two inputs NOR gate using CNTFET

B. PERFORMANCE ANLYSIS OF DIGITAL LOGIC CIRCUIT

We have to design the different digital logic gates simulation of these logic gates by using CNTFET. In Fig.7 shows the implementation of two-input NAND logic and Fig. 8 shows the implementation of two-input NOR logic circuits.

TABLE: I

Average Delay, Power, and Power-Delay-Product (PDP) For CNTFET Based Designs

Logic block	Power (J/s) (*1e-7)	Delay (s) (*1e-9)	PDP (J) (*1e-16)
Inverter	1.80	2.52	4.53
NAND	1.84	2.58	4.74
NOR	1.82	2.54	4.63

Table:1-performance analysis of digital logic circuit

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C. I-V CHRACTERISTICS OF CNTFET

The I-V characteristics of both type of CNTFET are obtained for 1.5 diameters, $R_{S/D}$= 75kΩ at room temp. (300k). In order to demonstrate the model we design the basic logic gates. The p-type and n-type characteristics is obtained when the P-G voltage is set on the -0.2v and n-type for +0.2.these types of Ambipolar CNTFET are used to design the circuit replacing by the traditional MOS transistor.

To perform the circuit we decided to use 900mv power supplies and flow band voltage are equal to +450mv and -450mv for both p-type and n-type characteristic curve shown in fig.

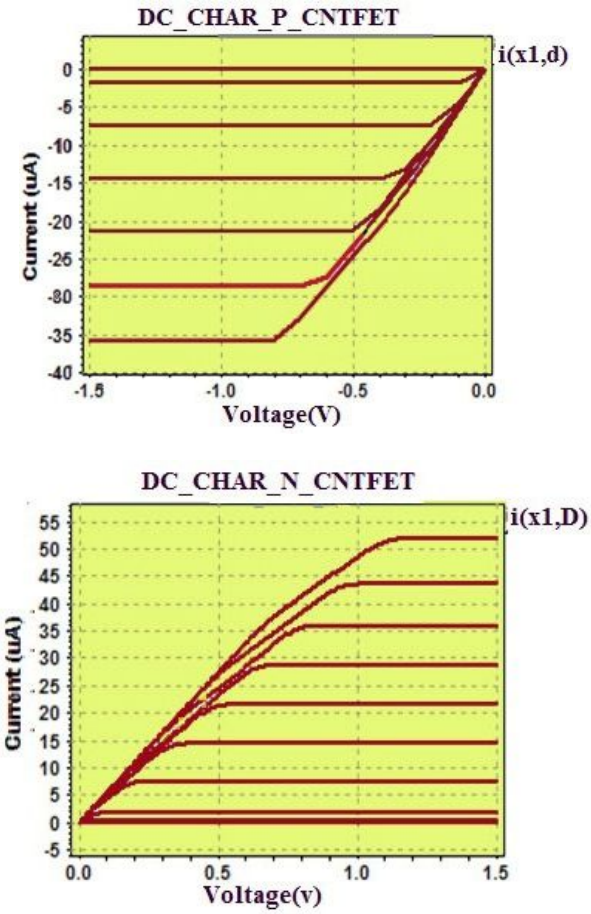

Fig.6: (a) ID- VDS characteristics of p-type CNTFET. (b) ID-VDS characteristics of n-type CNTFET. Parameters: d = 1.5 nm, RS/D = 75 kΩ, T = 300K.

IV. CONCLUSION

This paper has presented the design and analysis of the logic circuit based on CNTFETs. The threshold voltage of the CNTFET is function of the geometry of the CNTFET (i.e. the chirality). The major challenges faced by the CNFET are the presence of unwanted metallic tubes that has an unfavorable impact on the delay, power, and functional yield of carbon NanoTubes based circuits. Analysis of logic gates is performed using CNTFETs and comparison is done by changing various parameters.

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