[NC-Rase 18]
DOI: 10.5281/zenodo.1488731

ISSN 2348 – 8034
Impact Factor- 5.070

GLOBAL JOURNAL OF ENGINEERING SCIENCE AND RESEARCHES

EFFECT OF SCALING ON INTERCONNECT AND LOW-K INTEGRATION IN BEOL

Miss. Nanda V. Lanjulkar[*1], Prof. Nilesh M. Verulkar[2] & Dr. C. M. Jadhao[3]
[*1]PG Student, [2]Assistant Professor,[3]Professor & Principal
Department of Electronics &Telecommunication Engineering, Mauli Group of Institutions,
College of Engineering and Technology, Shegaon, Maharashtra, India

ABSTRACT

The introduction of various new materials and processes for fabrication of integrated circuit (IC) revaluated a semiconductor industry during last two decades. Such revolution in industry has been supported to shrink the device size beyond nano-region by increasing very packing density on single chip. However, scaling of device dimensions were introduces various serious reliability issues of interconnect and low-k materials in Back-End of Line (BEOL). Such interconnect related issues causes failure mechanisms on device performance and restrict the further scaling in device dimensions. But, very fast and small size devices are continuously demanded from society. Thus to fulfill the demand of society it is needed to understand the problem arises in BEOL and need more research to continue device scaling trend. This paper presents the details study of effect of scaling on interconnect and low-k. Also the problems arises during the fabrication in BEOL were also discussed in details.

Keywords: *scaling, low-k materials, BEOL.*

I. INTRODUCTION

The demand of small size, fast speed, high data rate and multicore processor has been fulfilled by reducing devices size towards nano region. However this continuous decreased in device sizes raised some material related issues in current technology. The problem related to interconnect and interlayer dielectric material (ILD) in BEOL attracted much more attention in order to continue this scaling trend. The reduction in spacing between interconnect arises the capacitance which increase RC delay, power dissipation and cross talk problems (1). The back-end-of line (BEOL) RC delay has gradually become a critical limiting factor in semiconductor circuit performance and causes the restriction for further scaling of device dimensions. Thus there is demand of new materials or new process technology. During 1990s, IBM introduces damascene process and further the dual damascene copper metallization processes developed in 1997 (2). The processes consist of patterning of line-space on ILD, CMP, spin-on antireflective coating, copper diffusion barrier, copper electroplating and polish (3-4). The need of new interconnect and interlayer dielectric (ILD) for future technology node was firstly were highlighted in Interconnect chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS). To connect the maximum number of devices with short interconnecting lines, the multilevel metallization (MLM) has been introduced. Integration and process issues in BEOL details described in ITRS 2014 (ITRS-2014). The problems occurred during integration of Cu/Low-k causes degradation of interconnect performance and k value (5). Leakge current and breakdown properties of low-k dielectric also observed to be reliability issues for interconnect (6). To overcome aforesaid reliability issues the aluminum (Al) metal layer has been replaced by copper (Cu) because of its low resistivity, but still there is no inevitable reduction in RC delay. Thus there is great demand of ILD material with ultra-low dialectic materials in future technology in order to further reduce the RC delay. The best way to lower the k value is to introduce the porosity in film matrix. But, to integrate a Cu/porous low-k post many challenges during integration in current technology. However, with positive impact such process raises reliability of interconnect and dielectric layer related issues in current technology. Using a low-k porous dielectric with a copper interconnect introduces several new challenges to reliability, including dielectric breakdown, temperature cycle, and stability within packages, resist poisoning, degradation of k value [7-8]. This paper highlighted the issues occurred in interconnect due to scaling of device size. Also need of low-k material is also illustrated in this paper.

ISSN 2348 – 8034
Impact Factor- 5.070

II. SCALNG IMPACT ON INTERCONNECTS

Interconnect playing an important role for distribution of clock signal and electrical power to the devices fabricated in FEOL with each other to make circuits for proper functioning. To separate this metal interconnects an interlayer dielectric (ILD) material is used. But as increase in devices density on a small area there is need to change an old process to cope up with new technology. Therefore a multilevel damascene structure was introduced in BEOL to integrate a metal wire and ILD materials. In this method metal lines are connected via holes to minimize wire lengths and interelectrode resistances and capacitances [5] The Figure 1 shows the cross section of multilevel interconnect structure [9].

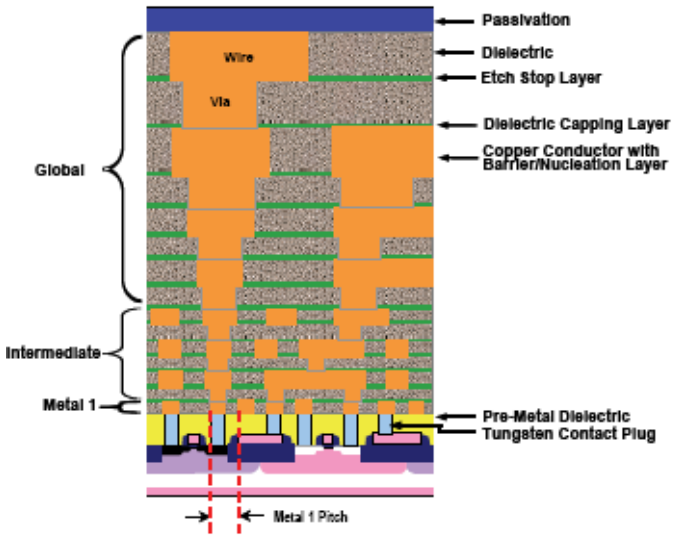

Figure 1: Cross-section of Hierarchical Scaling—MPU Device (ITRS -07)

A. RC delay and cross talk and power consumption

An interconnect is characterized by three elements Resistance (R), Capacitance (C), Inductance (L), known as interconnect parasitic elements (10). Due to scaling of devise dimensions on one hand resulted interconnect metal wiring getting closer in vertical and horizontal direction on a single chip on the other hand. Figure 2 shows the typical structure of metal interconnects.

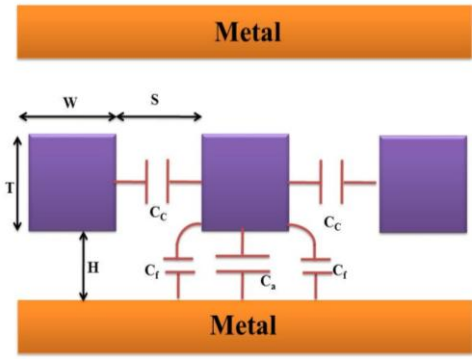

Figure 2: Typical metal interconnect structure

ISSN 2348 – 8034
Impact Factor- 5.070

$$R = \rho \frac{L}{WH} \qquad (1)$$

As integrated circuit devices shrinking continuously causes in rduction in spacing between metal wire i.e decrease in width (W), Height (H). Further to connect a high packing density devices without touching metal wires from each other, it was essential to increase the wire length. Increases in such metal wire length (L) leads to increase overall interconnect resistance as shown in equation 1 (Krishna Saraswat, Interconnet scaling).

$$C_{ILD} = K_{ox} \varepsilon_o \frac{WL}{X_{ox}} \qquad (2)$$

$$C_{IMD} = K_{ox} \varepsilon_o \frac{TL}{S} \qquad (3)$$

From equation 2 and 3 the capacitance depend on dielectric value (k), metal width (W), thickness (T), spacing between metal and thickness of dielectric (H). Scaling of these parameters leads to the increase in total interconnect capacitance. This causes the further increase in RC delay. To overcome these issues there is dire need to replace the metal wire material and dielectric material that are compatible with new process technology. Integration complexity The aluminium (Al) was already replace with low resistance copper (Cu) which help to reduce RC delay and improve the device performance.

$$P = \alpha CV2f \qquad (4)$$

Thereafter from equation 4 continuous power is proportional to density and operating frequency (f). Increase in device operating frequency and device density on single chip increases the power dissipation chip. The raises in power dissipation become a significant part of the overall power dissipated in the chip. The clock distribution and generation circuitry is known to consume average 50% of total power (11). Furthermore, as the interconnects are routed close to each other leads the signals on the lines can crosstalk to each other via near field electromagnetic coupling. Signal crosstalk is given by the ratio of line to line (sidewall) capacitance to total capacitance. Thus increase in total capacitnace due decreament in the feature size introduces higher crosstalk. Thus it is necessary to reduce the total interconnect capacitance. Thus to reduce line to line capacitance it is inevitable to use dielectrics with lower dielectric constant. Driver deep submicron technologies were reported to minimize an crosstalk noise (12). Sandeepsharma in his published paper reported the carbon nanotube (CNT) as an promising candidate for interconnect (13).

B. Electromigration

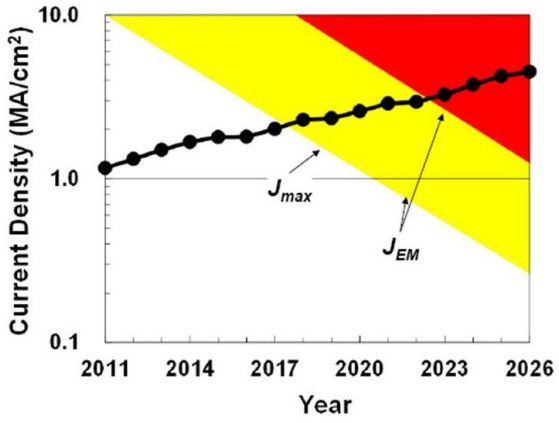

Figure 3: ITRS 2011 interconnect chapter Current density vs year (14)

ISSN 2348 – 8034
Impact Factor- 5.070

Electromigration (EM) is the transport of material caused by the moment of ions in metal. This EM phenomenon in the present era of increasing current densities is considered as a serious issue in the IC industry. The figure 3 shows the increase in current density with year (13). From figure the red region to indicate the EM issues becoming serious issues in future technology node. Also beyond 22 nm noe , feature size effects, such as electron scattering from grain boundaries and interfaces, will continue to increase the effective Cu resistivity (11). This increase of current density in a such very low interconnect line width leads to a local temperature rise around the void due to joule heating causes the current stress.

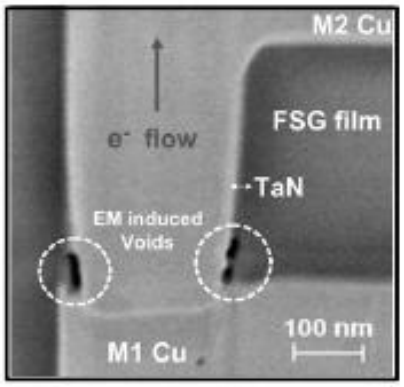

Figure 4: TEM cross sectional image showing EM induced voids (12)

This stress induced avoids in metal line which become a prime factor of electromigration in metal wire. (15) . As EM induce mass transformation through diffusion. This significant mass transfer creates voids in Cu metal which causes large increment in resistivity of interconnect metal. Cher Ming Tan and research group briefly reported on electropmigration in ULSI interconnects (16). Generation of void growth under the through silicon via(TSV) causes the change in resistance of metal interconnect (17).Electrical failure due to EM of interconnects in relatively short times resulted a circuit lifetime to an unacceptable level.

Hideya Matsuyama and high group reported the degeneration void in copper interconnect due stress migration phenomenon. (18). such defect may damage the metal wire. Shinya and his research group reported a formation of voids due to annealing in copper interconnect (19). Thermal strain also leads to the generation of voids (20). In addition to this metallic diffusion is also found to be serious issues in Cu interconnect. As Cu is rapidly diffused in to dielectric materials. To overcome this problem a barrier metal is needed to keep Cu from diffusing through the inter level dielectrics. Barrier materials used for Cu wiring must prevent its diffusion into the adjacent dielectric but in addition must form a suitable, high quality interface with Cu to limit vacancy diffusion and achieve acceptable electromigration lifetimes. TaN/Ta and Tin/Ta.

C. Integration process challenges in BEOL

In current technology during integration copper interconnect and ILD materials goes through different processes called as damascene method. Damascene process consists of both trenches and via patterned in a dielectric, barrier layer formation, low-k, and chemical mechanical planarization etc (8). All these steps are repetitive and which leads serious interconnects reliability issues and degradation of ILD material k value. The problems raised during these steps are described below. IN Dual Damascene Process Createsvies and lines by etching holes and trenches in the dielectric, and then depositing copper in both features. Secondly, the dielectric is etched according to the defined photoresist pattern, and then barrier layer is deposited

After metal barrier deposition and Cu plating, chemical mechanical polishing (CMP) were used for polishing interconnect metals to remove the excess Cu and part of the low-k. However the CMP has notable side effects which includes dielectric erosion, metal dishing. Further, the CMP is basically a frictional process; hence it generates a lot

ISSN 2348 – 8034
Impact Factor- 5.070

of heat and may produce hot spots, leading to cracks and delamination in film. Figure 5 shows the dishing and erosion formation in copper interconnect.

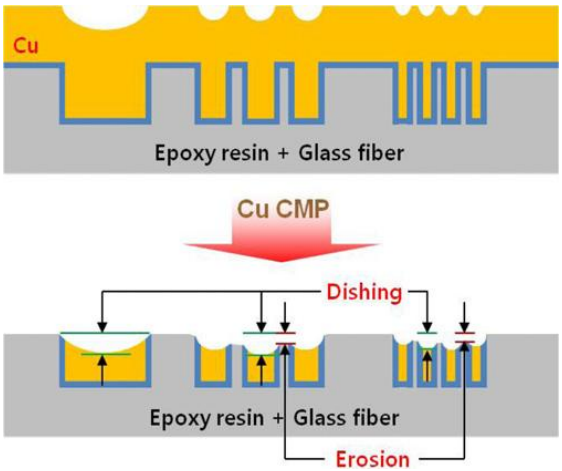

Figure 5: Generation of dishing and erosion during CMP (21)

In addition to interconnect CMP also raised mechanical issues in low-k films due to its lower mechanical strength. A typical mechanical failure mode includes delamination, cracking, and inelastic deformation in low-k films. Soocheon Jang and his group reported the dielectric erosion and Cu dishing after Cu CMP (19). Thus Copper chemical mechanical polishing (Cu CMP) is a critical process in the fabrication of high performance microprocessors and other advanced memory devices. (22). This undesirable effects resulted to degrade the process quality, cause significant yield losses in BEOL, and negatively affect interconnect performance, especially for wide global interconnects (23). Thus to improve the device performance it is needed to over this issues raised by CMP.

III. NEED OF LOW-K

As discussed earlier the performance of interconnect has been improved by replacing Al with Cu metal interconnect. Thus there is little scope to modify the conductivity of interconnects as copper has the lowest resistivity available of metals that are compatible with modern device processing. Therefore, RC delay can be reduced further only by lowering the capacitance through the use of dielectrics with lower k values. The traditionally used SiO2 as an ILD material has been replaced with lower k value porous low-k materials with k value <3. But as per the International Technology Road map for Semiconductor (ITRS) 2012 inter layer dielectric (ILD) materials which having k value < 2 is needed to bring the further device scaling in 45nm and beyond technology node.

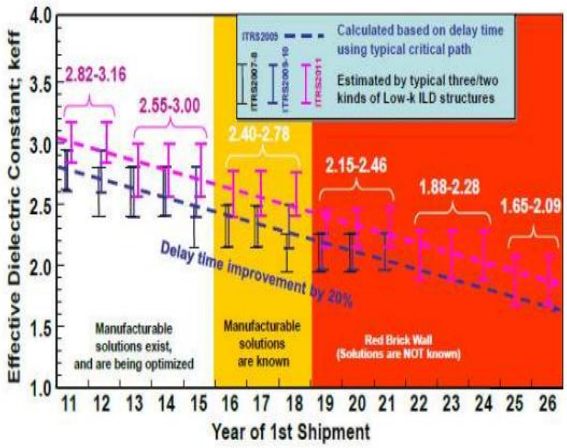

Figure 6 shows the requirement of low-k to reduce RC delay. To achieve lower k value the only options is to introduce the porosity in dielectric matrix structure. From the last decade researchers have put tremendous efforts towards the development of different low-k materials that can be implemented in industrial production. Silica aerogel have reported a lowest k value dielectric material as it has 99% porosity with lowest k value~1. But this porous nature of ILD material introduces number of reliability issues during integration in dual damascene structure. The issues included thin film cracking, delamination and thermal-mechanical reliability (24). Thus the porous low-k must have improved properties like high mechanical strength, hydrophobic nature in order to cope up with current technology. Improvements in porous low-k properties help to sustain during integration process and reduce the degradation of k value and reliability issues of interconnect. Rresearcher reported surface modification techniques to improve mechanical, thermal, thermal, electrical and making hydrophobic surface (8, 25). ITRS reported air gap ultimate solution to replace current ILD material. The air gaps provided 17% improvement in capacitance. Optical interconnect also reported a promising candidate for future technology node (26).

IV. CONCLUSION

This paper presents the impact of device scaling on the parameters of IC. It is observed that the scaling of device sizes causes the increase in RC delay and cross talk. These parameters becoming a primary design criterion due to its effects of device speed. Thus, to enhance the performance of the IC it is needed to reduce the capacitance by introducing ultra-low-k ILD material. Air gap or silica aergogel with lowest k value ~1 is becoming a suitable option as an ILD in future technology. Also, ppower dissipation is becoming important criterion in interconnect design hence need to find out a long term solution on it. In order to continue this scaling trend a long turn new design or process technology solution such as 3D IC, optical or carbon nanotube may helpful to overcome the problems arises in current technology. As EM is most effective to reduce device performance hence it is needed to reduce current crowding and optimization of barrier layer metal. Also continuing research is needed to understand the multi-variable nature of copper and low-κ interconnect reliability and provide accurate models for designed-in reliability. It is find out that better understand of the magnitude of the wire problem and interconnect constraints, better understanding of physical mechanisms of signal integrity and various design techniques at different design levels, are essential to the success of interconnect design. In addition to this the dimensional control and the resulting difficult challenge is getting a key challenge for present and future interconnect technology generations. Thus researcher getting challenges to development into new generations of copper and barrier processes.

REFERENCES

1. *PawanKapur, Gaurav Chandra, James P. McVittie, Technology and reliability constrained future copper interconnects-Part II: performance implications, IEEE Transaction on electronics devices, 49(4) , (2002), 598-604*
2. *D. Ang and R. V. Ramanujan, Hydrostatic stress and hydrostatic stress gradients in passivated copper interconnects, Material Science and Engineering, 423 (2006) 157-165*
3. *Copper interconnect technology by Tapan Gupta , Springer 2009*
4. *T.C. Wanga, Y.L. Wangb,c, T.E. Hsieha, S.C. Changb, Y.L. Chengb, Copper voids improvement for the copper dual damascene interconnection process, Journal of Physics and Chemistry of Solids 69 (2008) 566–571.*
5. *Chun-Jen Weng, Novel Approach of Semiconductor BEOL Processes Integration, Proceedings of the XIth International Congress and Exposition June 2-5, 2008 Orlando, Florida USA*
6. *Chi Kyu Choi , Chang Young Kim, R. Navamathavan, HeangSeuk Lee, Jong-Kwan Woo, MyungTaek Hyun, HeonJu Lee, Won Young Jeung, UV irradiation effects on the bonding structure and electrical properties of ultra low-k SiOC(eH) thin films for 45 nm technology node, Current Applied Physics 11 (2011) S109-S113*
7. *Mahadevaiyer Krishnan, Jakub W. Nalaskowski, and Lee M. Cook, Chemical Mechanical Planarization: Slurry Chemistry, Materials, and Mechanisms, Chem. Rev., 110, (2010)178–204178*
8. *Yogesh S. Mhaisagar, Anil S. Gaikwad, Anil G. Khairnar and A.M. Mahajan, Enhancement in Mechanical Properties of Silica low-k thin films by using Wet Chemical Techniques, Indian Journal of Pure and Applied Physics, 54, 439-442 (2016)*
9. *International Technology Roadmap for Semiconductor (ITRS) , Interconnect chapter 2007*

ISSN 2348 – 8034
Impact Factor- 5.070

10. *David Duarte, Vijaykrishnan Narayanan and Mary Jane Irwin,Impact of Technology Scaling in the Clock System Power, e Proceedings of the IEEE Computer Society Annual Symposium on VLSI, April 25-26, 2002, Pittsburgh, PA.*
11. *Kalpana.A.B, P.V.Hunagund, Effect of Driver Strength on Crosstalk in Global Interconnects (IJACSA) International Journal of Advanced Computer Science and Applications, Vol. 3, No. 9, 2012.*
12. *Sandeep Sharma, RajeevanChandel, Pankaj Kr. Pal, Rituraj S. Rathore, Performance Analysis of CNTs as an Application for Future VLSI Interconnects , Microelectronics and Solid State Electronics 2012, 1(3): 69-73*
13. *International Technology Roadmap for Semiconductor (ITRS),Interconnect chapter (2011).*
14. *Y. L. Hsu, Y. K. Fang,z Y. T. Chiang, S. F. Chen, C. Y. Lin, T. H. Chou, and S. H. Chang, Failure Mechanism of Electromigration in Via Sidewall for Copper Dual Damascene Interconnection, Journal of The Electrochemical Society, 153 _8_ G782-G786 _2006.*
15. *Md. KhalilurRahman, AbulMonsur Mohammed Musa, BudrunNeher, Kawchar Ahmed Patwary, Mohammad AtiqurRahman, Md. Shariful Islam, A Review of the Study on the Electromigration and Power Electronics, Journal of Electronics Cooling and Thermal Control, 2016, 6, 19-31*
16. *Cher Ming Tan and ArjitRoy,Electropmigration in ULSI interconnects, Materials Science and Engineering R Reports, 58 (1-2), 2007*
17. *R.L. de Orio,H. Ceric, and S. Selberherr,.Electromigration failure in a copper dual-damascene structure with a through silicon via, MicroelectronReliab, 52(9-10)2012 1981–1986.*
18. *Seiichi Kondo, Yasuhiro Ichige and YuyaOtsuka,Advanced metallization for ULSI applications,Japanese journal of applied physics, 56 (7S2), 2017*
19. *Effect of annealing atmosphere on Void formation in copper interconnest , Shinya Konishi, Miki Mpriyama and Masanori Murkami, Materials Transactions, 43 (7), 2002, 1624-1628*
20. *Iournal of Applied Physics, 98, 2005, 07451-1-8*
21. *Soocheon Jang, HaedoJeon, MinjongYuh, and Jaehong Park, International Journal Of Precision Engineering And Manufacturing-Green Technology, 2(1)(2015) 59-63*
22. *M.KrishnanM.F.Lofaro, Copper chemical mechanical planarization (Cu CMP) challenges in 22 nm back-end-of-line (BEOL) and beyond, Advances in Chemical Mechanical Planarization (CMP) 92016) Pages 27-46*
23. *Runzi Chang, d Costas J. Spanos Modeling the Electrical Effects of Metal Dishing Due to CMP for On-Chip Interconnect Optimization, IEEE Transactions On Electron Devices, 51(10), 2004*
24. *W. Zhou,1 S. Bailey,1,a) R. Sooryakumar,1 S. King,2 G. Xu,2 E. Mays,2 C. Ege,2 and J. Bielefeld2, W. Zhou,1 S. Bailey,1,a) R. Sooryakumar,1 S. King,2 G. Xu,2 E. Mays,2 C. Ege,2and J. Bielefeld2, JOURNAL OF APPLIED PHYSICS 110,(2011) 043520*
25. *Chi Kyu Choi , Chang Young Kim , R. Navamathavan, HeangSeuk Lee , Jong-Kwan Woo, MyungTaek Hyun , HeonJu Lee , Won Young Jeung, UV irradiation effects on the bonding structure and electrical properties of ultra low-k SiOC(eH) thin films for 45 nm technology node, Current Applied Physics 11 (2011) S109eS113.*
26. *David A. B. Miller ,Optical interconnects to electronic chips, Applied Optics, 49(25 / 1) (2010) F59-F70.*