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PERFORMANCE ANALYSIS OF MULTI-LEVEL INVERTER WITH LCL FILTER FOR PV SYSTEM

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ABSTRACT

The purpose of this study is to detail a five-level inverter architecture that utilises three phases for the purposes of photovoltaic system usage. In this article, a three-phase 30 kW, five-level diode-clamped inverter output is filtered using an LCL filter. In this paper, the phase disposition pulse width modulation technique (PDPWM) is utilised to manage the switching states. This system has been created using MATLAB/Simulink simulations with two cases: one is when the system is connected to the grid, and the other is when it is independent. The inverter produces a sinusoidal 400 V three-phase voltage that is then filtered and used to inject power into a resistive load and the grid. A harmonic distortion level of 22.53% is found without a low-pass filter, whereas with a filter, the harmonic distortion was 3.07%. The THD for the grid-connected example is 4.86% with an LCL filter. The proposed topology and filter design in the simulation have been proven to generate a minimum tolerable harmonic level in line with IEEE:519-2014.

Keywords*: LCL Filter, Multi-level Inverter, PDPWM, Solar Energy, THD.*

I. INTRODUCTION

Applying renewable energy sources is effective approach to use solar photovoltaic (PV) power plants. Solar PV modules produce a relatively low voltage DC source that converts light into electrical energy, and the modules have low conversion efficiency [1]. Multi-level inverters are in particular among the kinds of devices employed to supply the power from the photovoltaic system to the load or the grid.

A. Related Work

There are many writers who have submitted articles that look at multi-level inverters equipped with LCL filters for PV systems. Xiaoqiang Guo et al. [2] put forth a new multi-level inverter (MLI) that is made specifically for PV power plants. They concluded that the five-level inverter produces an alternating wave with switching states. The idea of a single-phase MLI (Modular Low-Tension Inverter) is presented in [3] to power stand-alone PV systems. That research article uses micro MLI structure for smaller loads. A single-phase MLI with PV panel integration was created in [4]. The researchers proposed and studied a half bridge inverter circuit being combined with a standard cascaded H-bridge MLI.

The research involving three-phase MLI is particularly important, as most research in the past is attentive towards single-phase claims. Owing to the ability in making it possible to build a better voltage waveform regarding increased harmonic range, it is best suited for applications that have a greater voltage. They can obtain higher voltages with limited maximum device ratings.

Inverters connected to the grid, a filter seems essential as a harmonic compensator between the inverter and the grid. In [8], the authors proposed LCL filter for grid-connected three-phase inverter. Based on their findings, the most effective filter for suppressing of the harmonics occurring from the switching frequency injected into the grid is the LCL filter.

B. Contribution of Paper

This study explores how to design and undertake a presentation examination of a three-phase multi-level inverter for use in a PV system. To control harmonic distortion, a three-phase clamped-inverter architecture equipped with

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PDPWM control and LCL filtering will be supplied

C. Organization of Paper

The document is laid out in this way: Section 2 reports the design of the suggested system; section 3 presents LCL filter design, using a controlled technique. Section 4 addresses simulation results. Finally, section 5 draws the conclusion on the basis of the simulation results.

II. PROPOSED SYSTEM

Figure 1 shows the general design of the PV system with the multi-level inverter layout. The multi-level inverter with LCL filtering has five-level output, and it injects power to the load. Every section of the line diagram is discoursed unconnectedly.

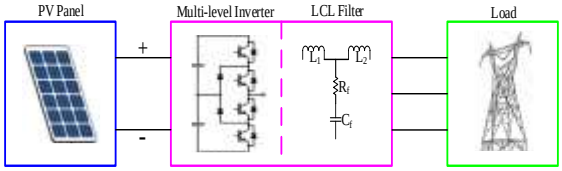

Figure 1. Line diagram of proposed PV system

A. Modelling of PV

PV array seemed to designed by assembling relating PV cell connected within sequences or parallel. Since power engendered by PV cell appears very small, it is required to consider cumulative output power. Thus, PV cells are connected in series or parallel forming PV array. Required equations for PV array [9] are as follows.

$$\text{Ah to load} = I_R \times \text{Peak sun hours} \times \text{Coulomb efficiency} \times \text{De-rating factor} \quad (1)$$

$$\text{Total load(Ah/day)} = \frac{\text{Total DC load}(\frac{\text{Wh}}{\text{day}})}{\text{System voltage(V)}} \quad (2)$$

$$\text{Module in series} = \frac{\text{System voltage}}{\text{Nominal voltage}} \quad (3)$$

$$\text{Strings in parallel} = \frac{\text{Ah/day}}{\text{Ah/day per module}} \quad (4)$$

Through (1) to (4), the value of module in series and strings in parallel can be achieved. De-rating element about 10% is taken to account for dirt and gradual aging of modules. For estimation, an over all inverter efficiency of about 85 % is considered to be a conservative default assumption. The total ratings for proposed PV system are summarized in Table 1.

Table 1. Total Rating for Proposed PV System

Sr No.	Parameter	Symbols	Value	Units
1.	Total rating	P	30	kW
2.	Series number of PV	-	11	Nos
3.	Parallel number of PV	-	9	Nos
4.	Output PV voltage	V	600	V

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Table 1 shows that total power 30 kW produced from PV (11 numbers of series and 9 numbers of parallel connection). Nevertheless, supreme energy for one PV module seems 54.7 V, energy has been augmented to 600 V by linking series 11 numbers and current has been amplified to 50 A by linking parallel 9 numbers. Apollo Solar Energy ASEC-305 G6S Solar PV panels [10] had been chosen for PV model.

B. Multi-level Inverter

A significant role played by an inverter is that it converts the DC voltage generated by a photovoltaic system to an AC voltage to be sent into the grid. The H-bridge cascade inverter is a type of multi-level topology that is common and includes the flying capacitor and diode-clamped inverters. In this research, the three-phase diode-clamped multi-level inverter is used. The alternating high and low incidences regarding blinking high and low frequencies of diode-clamped inverters help these structures operate. There are multiple sorts of modulation algorithms in use for creating multi-level inverter switch switching pulses. The PWM approach has numerous triangular carrier waveforms, each of which is utilized in producing substituting pulses having sinusoidal reference [11]. The pulse width modulation approach is important towards inverter because it provides pulse signals that the switches need to open and close and so provide the required output voltage [3]. Of the various kinds of multi-level modulation, the general application of three kinds of carrier disposition PWM modulation may be classified into PD, POD, and APOD [12]. This paper will concentrate on the PDPWM in order to make multi-level inverter modulation simpler.

C. LCL Filter

To combat current and voltage harmonics, LCL filters were specifically developed for power converters. In general, these units have parallel-series reactor and capacitor configurations that are customised to minimise THD. The LCL filter is more effective in lowering switching harmonics than the L filter and LC filter. [13] states that it works with lower switching frequency and voltage loss. Instead of using the L filter, which tends to be less precise, a high-order LCL filter was applied to make the multi-level inverter's output voltage sinusoidal.

D. Load

The load is analyzed two compartiments

Case 1 : The three-phase resistive load is connected to the stand-alone PV system.

Case 2 : Three-phase multi-level inverter connected to the 20kW load and to 400V

III. PULSE WIDTH MODULATION STRATEGY AND FILTER DESIGN

A. Control Scheme for Multi-level Inverter

For three-phase inverters, gate pulse signals have been engendered consequently in comparison with 3 sinusoidal reference indications concerning shipper indications. production voltage is measured fluctuating modulation index (MI) worth aimed at dissimilar breadth concerning orientation indications. For N-level inverter (N-1) carrier signals have been mandatory. In undertaken research, 4 carrier signals seemed twisted for afive-level inverter. MI is measured applying following equation [5]:

$$\text{Modulation Index} = \frac{2\times A_m}{(N-1)\times A_c} \quad (5)$$

where,

Am is largeness of reference signal and Ac is peak to peak value of carrier signal.

For five-level inverter, four carrier signals have been compulsory, 2 located above zero level and other two signals sited below zero level. The S is the number of DC sources required for the number of output voltage level (N) is intended applying following equation.

$$\text{Nlevel} = [(2\times S)+1] \quad (6)$$

If S=2, output waveform will have five-level. Number of switches and diodes applyed within topology appears calculated applying equations (7) and (8), respectively.

$$\text{Mswitch} = 6(m-1) \quad (7)$$

If m = 5, Mswitch=24

$$\text{Mdiode} = 3(m-1)(m-2) \quad (8)$$

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If m = 5, M_{diode}=36

The schematic diagram of PDPWM control scheme is shown in Figure 2.

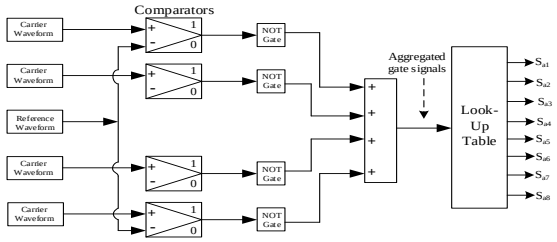

Figure 2. Schematic diagram of control scheme

To regulate a multi-level inverter, the PDPWM technique is utilised. As the carrier waveform, triangular waveforms are used as reference waveforms in the 50 Hz line frequency. Output voltage THD and switching losses can be reduced by setting MI=1. The frequency applied to the carrier waveform is 500 Hz, which is low, but the THD is also low. Each group within network has been fashioned by identical amount regarding carrier indications: higher ones within Upper group and lower ones within lower collection. upper- and lower-layer carriers have been positioned upon contradictory sides of zero, higher carriers are above zero (positive) and lower carriers are below zero (negative) (negative side).

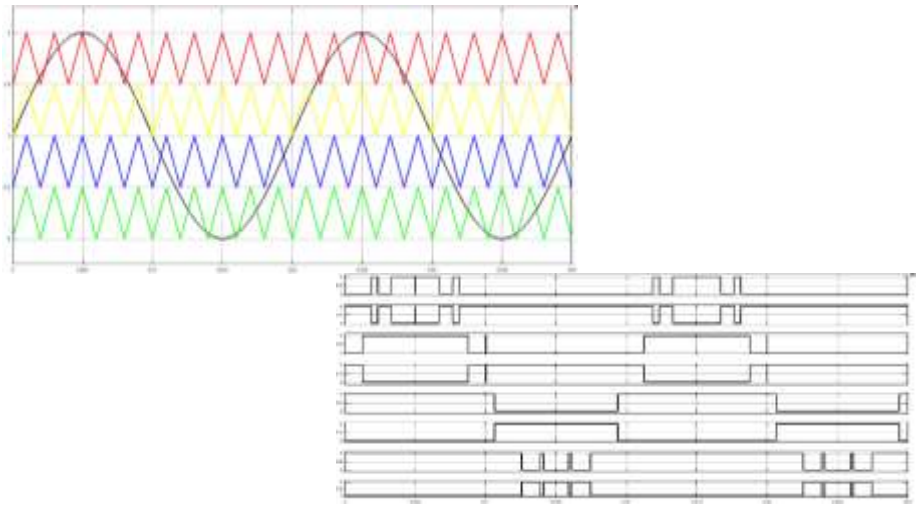

Figure 3. Reference, carrier and cumulative gate signals

The gate pulse signals can be seen in Figure 3. Because of three-phase five-level inverter, there will be eight switching states.

These gate pulses are represented switching states. As one pair of eight switching states, S_{a1} is ON when S_{a2} is OFF. Other switching states will be the same as these switch pairs. The functions of these eight switches can be seen in that figure.

B. LCL Filter Design

Figure 4 shows an LCL filter connecting the MLI to the grid. inverter side inductor L1's existing ripple seems strongminded by capacitor voltage and inverter output voltage. Locations concerning LCL filter have been partial by design boundaries to twitch with specific limits in place. Bigger inductance seems desirable within L1 because of its miniature existing ripple. To lessening ripple at high frequencies, intensification the capacitor's value. L2, the grid side inductor, can serve to smooth out the harmonic noise. The current induction on the L1, inverter side is essential

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for the filter design as it is a fundamental component that connects the power stage of the inverter to the grid. Choosing because it works well at low switching frequencies is the most critical factor. Here's how the design equations are expressed.

Figure 4. Schematic diagram of Grid connected LCL filter

$$Zb = (En)2/P \quad (9)$$

$$Cb = 1/\omega g \times Zb \quad (10)$$

$$Imax = \sqrt{2}\ P/3 \times Vf \quad (11)$$

where, E_n is one phase effective voltage, P is active power, Cb appears base capacitance, ωg is grid angular velocity, Zb is base impedance, and Vf is filter voltage.

If the rated current is allowable to fluctuate by 10% for the design parameters, the values in (12) and (13) are obtained.

$$\Delta I_{l-max} = 0.1 \times I_{max} \quad (12)$$

$$L_1 = \frac{V_{DC}}{6 \times f_{sw} \times \Delta I_{l-max}} \quad (13)$$

where, L1 is inverter side inductance, fsw is switching frequency, and VDC is DC link voltage.

Inverter side inductor is greater than grid side inductor and switching frequency is 10 times of carrier frequency. The capacitor and grid side inductor L2 is designed based on attenuation factor. The capacitor value is limited by the reduction of the power factor(less than 5%) in the rated capacity. The capacitance value, the attenuation factor, the resonance frequency are given by (15) and (18).

$$Cf = 0.05 \times Cb \quad (14)$$

$$k_a = 0.2(20\%) \rightarrow \text{attenuation factor} \quad (15)$$

$$L_2 = \frac{\sqrt{\frac{1}{k_a^2}} + 1}{C_f \times \omega_{sw}^2} \quad (16)$$

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 \times L_2 \times C_f}} \quad (17)$$

$$f_{res} = \frac{\omega_{res}}{2\pi} \quad (18)$$

where, Cf is filter capacitance, L2 is grid side inductance, ωres is resonance angular velocity, fres is resonance frequency.

To avoid resonance, diminish a part of ripple at swapping frequency, resistor associated series regarding capacitor seems required. This resistor are up towards one third of filter capacitor impedance at resonance frequency rated. Filter resistance value can be expressed as.

$$R_f = \frac{1}{3 \times C_f \times \omega_{res}} \quad (19)$$

where, R_f is filter resistor, C_f seemse filter capacitor and ω_{res} is resonance angular velocity.

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IV. SIMULATION RESULTS AND DISCUSSION

Figure 5 shows Simulink diagram of proposed system. The parameters to be used in the simulation model are summarized in Table 2.

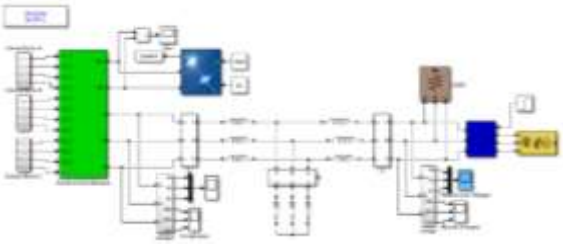

Figure 5. MATLAB/Simulink circuit modeling

Table 2. Parameters used in Simulation Study

Sr No.	Parameter	Symbols	Value	Units
1.	Phase-phase voltage	E_n	230	V
2.	Grid frequency	F_g	50	Hz
3.	Active power	P	20	kW
4.	Switching frequency	F_{sw}	5	kHz
5.	DC link voltage	V_{DC}	600	V
6.	Inverter side inductor	L_1	84.85	mH
7.	Grid side inductor	L_2	8.43	mH
8.	Filter resistor	R_f	3.73	Ω
9.	Filter capacitor	C_f	61.245	µF
10.	DC link capacitor	C_{DC}	2835.5	µF

In SimPower Systems of MATLAB/Simulink, the simulink circuit is utilised. The three-phase five-level diode clamped inverter block is used within conjunction with an LCL filter design and a PV block in the system. These two instances indicated in section 2.4 have been tried with simulation results. A MATLAB/FFT spectrum analysis is used in powergui's spectrum analysis window to investigate line voltage harmonics.

A. PV Array Characteristics

Two key variables, irradiation and temperature, affect voltage PV system. Sun radiation causes output current change, temperature causes terminal voltage change. In Figure 6, you can see that I-V(Current-Voltage), P-V(Power-Voltage) characteristics PV module (with cell temperature held constant at 25 ˚C) experience greater fluctuation in solar radiation levels. 1000 W/m2, 800 W/m2, 700 W/m2 are used for various irradiation values.

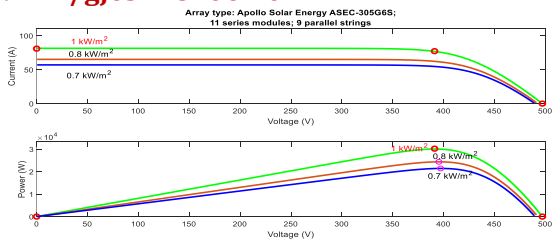

Figure 6. I-V & P-V Characteristics curve of the solar PV panel with variable irradiation

Figure 7. shows the I-V(Current-Voltage) and P-V(Power-Voltage) characteristics of the PV module under varying cell temperature at constant solar radiation (1000 W/m^2). The panel temperature is varied by setting three values 25°C, 45°C and 55°C, respectively.

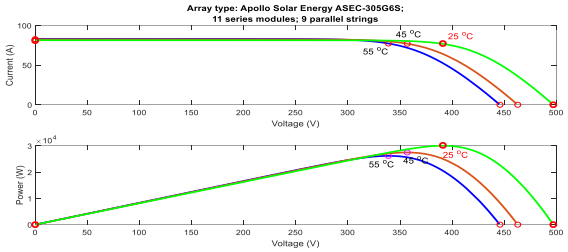

Figure 7. I-V & P-V Characteristics curve of the solar PV panel with variable panel temperature

To acquire 1000 W/m2 rating, one of the radiation values needs to be 1000 W/m2. The desired rating is achieved with the standard temperature of 25 degrees Celsius. The panel utilised for the investigation was the Apollo Solar Energy ASEC-305 G6S with settings of 25°C and 1000 W/m2, respectively.

B. Simulation Results and Discussion

Simulations were performed using the parameters specified in Table 2 using a MATLAB/Simulink simulation of the proposed PV system with a resistive load and grid-connected condition.

Case 1: Stand-alone System

In Figure 8, the three-phase five-level diode-clamped inverter output line voltages applying using PDPWM technique are displayed in stand-alone situation with 20 kW resistive load. From the diagram, you can see that the voltage output waveform has five steps before filtering. Voltage measurements have ranged from 0V to ±500V (±750VDC). Figure 9 shows the line current waveforms. The LCL filter will remove significant THD from the sinusoidal output waveforms, because the LCL filter was designed to take away THD.

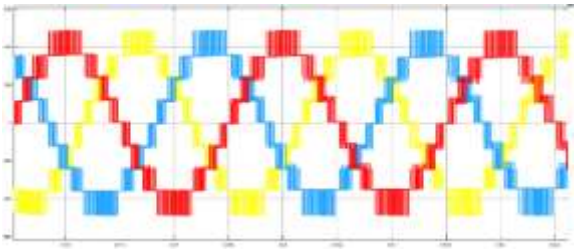

Figure 8. Output voltage waveform of five level inverter without filter

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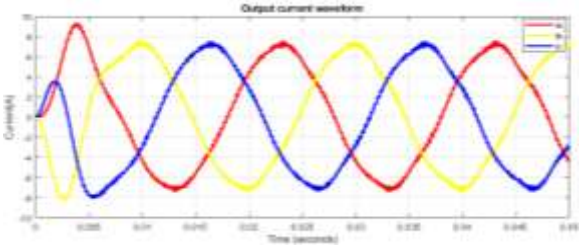

Figure 9. Output current waveform of five-level inverter without filter

Figure 10 depicts the FFT analysis of the inverter output voltage prior to LCL filtration. The fundamental content of the voltage at 50 Hz is 223.6 with a THD of 22.59 percent when it's without the LCL filter. Table 3 lists the harmonic orders that apply to the inverter output voltage. You should always filter the material before putting it into the load. The line current and output voltage waveforms from the system with the planned LCL filter are illustrated in Figures 11 and 12. When the AC 400 V comes out of the Simulink/FFT block, it will be linked to the load and examined for THD percent. To determine how effective the filtering is, a THD percent measurement is done on a previous measurement and one after filtering.

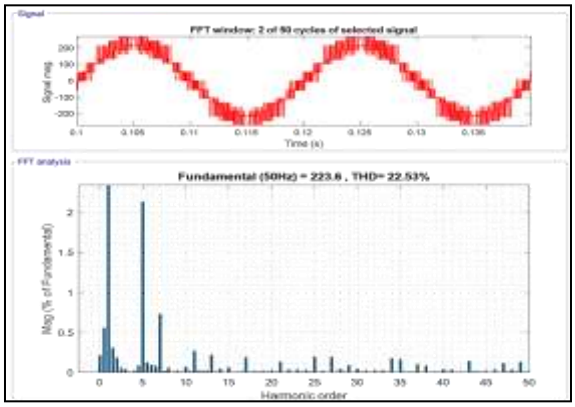

Figure 10. THD% of three phase stand-alone five-level inverter without filter

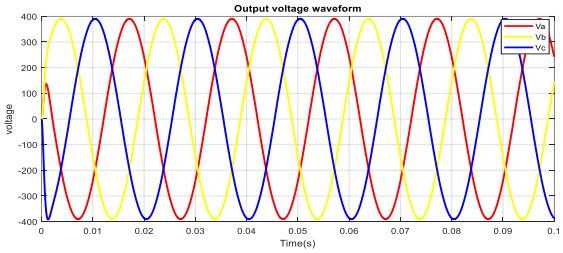

Figure 11. Output voltage waveform of five level inverter with filter

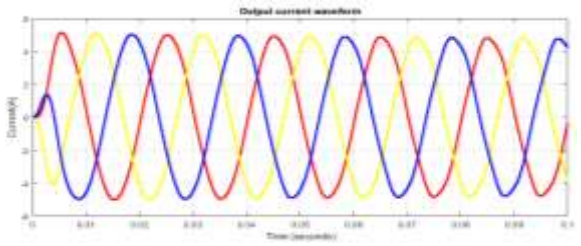

Figure 12. Output current waveform of five-level inverter with LCL filter

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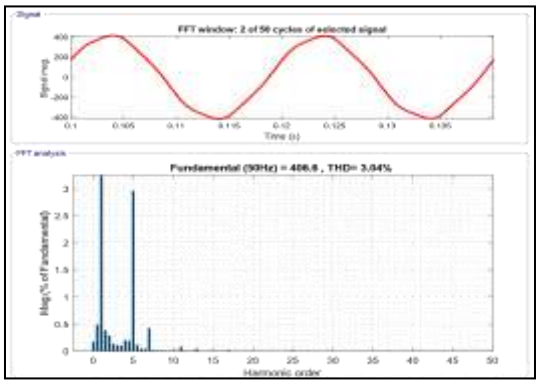

Figure 13. THD% of three phase stand-alone five level inverter with LCL filter

The voltages, which have passed through the LCL filter, will be smooth-shaven after removing the high frequency harmonics. Figure 13 shows the results of FFT analysis of output line voltage (400 V) of the RL load (20 kW) on the stand-alone system, which is targeting modulation index=1. The basic content of the FFT of the voltage waveform of the converter is 406.6 at 50 Hz with a 3.04% FFT result. Based on the THD results, the report concludes that the 9th harmonic is below 8% according to IEEE 519-2014 standards [16]. Compared to the step output waveform of Figure 8, the THD of the output voltage in the first example is low in magnitude.

Table 3. Harmonic Distortion of three phase five-level stand-alone inverter

System	Individual Harmonic Voltage Distortion (%)						
	5th Order	11th Order	23rd Order	33rd Order	41st Order	49th Order	THD (%)
Without Filter	3.93	0.68	0.11	0.05	0.07	0.23	22.53
With LCL Filter	2.97	0.11	0.02	0.01	0.01	0.01	3.07

The comparative assessment of harmonic voltage distortion levels with and without LCL filter is summarized in Table 3. According to the Table, the THD of the voltage without filter lies above the specification of IEEE:519-2014. Although the individual voltage harmonics are less than 5%, the total THD is 22.53 %, which is much more than 8% standard. With LCL filter, all the individual voltage harmonics are less than 5% as well as the total THD is 3.07% (less than 8% standard). Therefore, the five-level MLI with LCL filter supporting the PDPWM switching technique will be effectively applied in the PV application.

Case 2: Grid-connected System

For grid-connected case, the PV system parameter, the inverter topologies and control strategy, and the designed LCL parameter are the same system as likewise the stand-alone case. But, the AC source considering as grid utility is connected through three-phase breaker.

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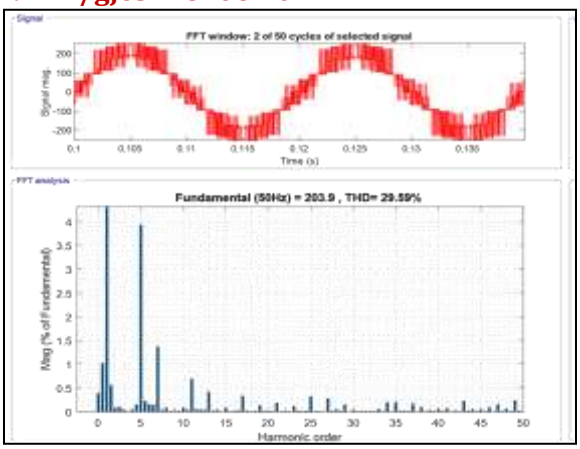

Figure 14. THD% of three phase grid connected five level inverter without filter

The output line voltage for three phase resistive load (20 kW), to 400 V three-phase grid in Figure 14 has been observed with Simulink/FFT analysis. In this case 2, the grid connected system also uses modulation index value of 1 and PDPWM method.

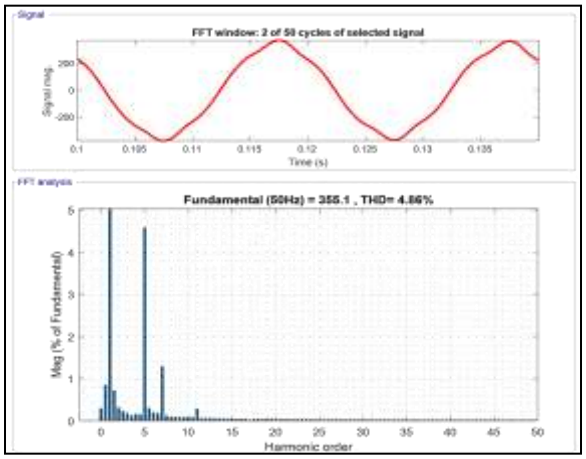

Figure 15. THD% of three phase grid connected five level inverter with LCL filter

The THD (total harmonic distortion) of the output line voltage waveform from the PDPWM technique is 29.59 percent. The input for the load includes both AC source and PV source, which decreases the fundamental content by 203.9. Figure 15 shows suggested system of LCL filter having signal pane and FFT analysis pane. To evaluate, summarise individual voltage harmonics and overall THD having and not having LCL filter, both have been tested.

Table 4. Harmonic Distortion of three-phase five-level grid connected inverter

System	Individual Harmonic Voltage Distortion (%)						THD (%)
	5th Order	11th Order	23rd Order	33rd Order	41st Order	49th Order	

Without Filter	3.93	0.68	0.11	0.05	0.07	0.23	29.59
With LCL Filter	4.57	0.28	0.03	0.02	0.01	0.01	4.86

As observed in the table, with and without a filter, the individual voltage harmonic distortions are 5% or less. Though 8 percent is still below, the overall THD of without a filter is 29.59 percent, making it a more than satisfactory figure. The LCL filter ensures the THD is below the target range (4.86%), as opposed to 8%. LCL filter results in virtually sinusoidal converter output in the simulation. The LCL filter enables superior output profiles, and it is possible to meet THD to IEEE:519-2014-defined acceptable limits. It is confirmed that the LCL filter is an appropriate option for linking the proposed system to the power grid.

V. CONCLUSION

With this document, you can see how the five-level, three-phase, diode-clamped inverter with an LCL filter does in relation to total harmonic distortion, whether the system is linked to the grid or on its own. This paper presents a MATLAB/Simulink based investigation of PDPWM control technique and LCL filter design. Results have been shown for the DC link voltages, inverter output, and percent THD of the stand-alone inverter and grid-connected inverter simulations. Using phase disposition pulse width modulation (PDPWM), a multi-level inverter with three-phase five-level diode-clamped power devices was investigated. Case studies both utilise the modulation index (MI=1). Using MATLAB/Simulink, the results demonstrate that the PDPWM technique has a better performance in terms of output voltage harmonic distortion, because it reduces harmonic distortion of individual voltage harmonics as well as the total THD. The system outperforms IEEE:519-output 2014's quality and THD percent, based on the results. The new system consisting of three-phase, five-level inverters with LCL filters may be run off the main utility grid, and it will be able to do so in an efficient manner.

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